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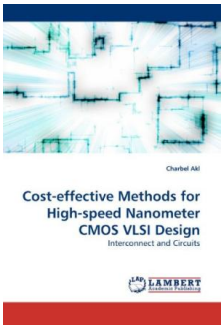
COST-EFFECTIVE METHODS FOR HIGH-SPEED NANOMETER CMOS VLSI DESIGN



Condition: New. Publisher/Verlag: LAP Lambert Academic Publishing | Interconnect and Circuits | The semiconductor industry has been following Moore s law over the past five decades due to the continuous CMOS process technology scaling. This scaling has led to reduced integrated circuit cost, higher integration density and better design performance. On the other hand, many new design challenges have been introduced due to scaling, and these chanllenges become more significant when migrating from one technology node to a newer one...

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